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MHKKG/SUN
P.O. BOX 398
AUSTIN, TX 78767

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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 10/817,632
Filing Date: April 02, 2004
Appellant(s): LANDIN ET AL.

Erik A. Heter
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed 8/3/2007 appealing from the Office action mailed 10/20/2006.

(1) Real Party in interest

A statement identifying by name the real party interest is contained in the brief.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The statement of the status of claims contained in the brief is correct.

(4) Status of Amendments After Final

The statement of the status of claims contained in the brief is corrected

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection to be reviewed on appeal is correct.

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

US 5940870	Chi et al	8-1999
US 6678799	Ang	1-2004
US 2002/0112124	Arimili et al	8-2002

(9) Grounds of Rejection

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-5,7-8,10-14,16-20 rejected under 35 U.S.C. 103(a) as being unpatentable over Chi et al (US 5940870) in view of Ang (US 6678799).

As in claim 1, Chi A system, comprising: a plurality of nodes, wherein each node includes an active device and a memory subsystem coupled to the active device (Chi's Fig 4: memory subsystem, #54 cluster cache, #43 memory controller, #62 private memory, #64 global memory) ; wherein an active device in a node of the plurality of nodes is configured to generate a global address and translation information identifying a translation function (Chi's Fig 8: device configured to generate global address), wherein the global address identifies a coherency unit (global address is used to identify coherency memories in nodes);

wherein a memory subsystem included in the node is configured to perform the translation function identified by the translation information on the global address to generate a physical address of the coherency unit within the memory subsystem (Chi's Fig 8, global address

is used by the destination node to generate physical address of physical memories in destination node, Fig 7 further shows the mapping to destination node physical memory #100);

wherein an additional memory subsystem included in an additional node of the plurality of nodes is configured to store the translation information identifying the translation function used in the node (Chi's Fig 8, column 5 lines 27-46 discloses data structures in each node to store the translation information that identifying the translation function used in each node, such as Fig 8: node ID #114, #110 partition number, ATM tables and indexes), wherein in response to a request for access to the coherency unit, the additional memory subsystem is configured to send the translation information to the node.

Chi's column 6 lines 21-25 discloses that a transaction packet including information in the global address such as the "translation information" (Chi's Fig 8: node ID, Partition, ATM indexes) destined to another node is generated and sent to a remote/destination node. Chi does not expressly disclose the claim's aspect of the additional memory subsystem is configured to send the translation information to the node. However, Ang's column 5 lines 27-30 discloses a distributed shared cached memory system in multiple nodes (Fig 1), in which the home node (Ang's Fig2: node 3) for a coherency unit has a directory keep tracks all necessary meta data and status for a cache line. When a request/packet for a cache line arrived, the home node's directory is consulted, and the home node (corresponding the claim's another node) sends out the response packet, including the address and node ID identifying the location an the manner the data being cached (Ang's column 5 lines 19-26). It would have been obvious to one of ordinary skill in the art at the time of invention to include the home node as suggested by Ang in Chi's system thereby the location and manner of data being cached car readily provided by the home node in

the situation wherein the data is not cached at the requesting node (Ang's column 5 lines 13-21; 27-36).

As in claim 2, the claim recites wherein the plurality of nodes are coupled by an inter-node network, and wherein each of the plurality of nodes includes an interface to the inter-node network (Chi's Fig 1: #20 internode network); wherein an additional interface included in the additional node is configured to receive the translation information for the coherency unit from the additional memory subsystem (Chi's Fig 8 shows destination node receiving the translation information for a coherence memory cached data) ;

wherein the additional interface is configured to provide the translation information and the global address to an interface included in the node via the inter-node network; and wherein the interface included in the node is configured to provide the translation information and the global address received via the inter-node network to the memory subsystem. The claim rejected based on the same rationale of claim 1 (Aug further discloses the home node's directory is consulted, and the home node (corresponding the claim's another node) sends out the response packet, including the address and node ID identifying the location an the manner the data being cached (Ang's column 5 lines 19-26)).

As in claim 3, the claim recites wherein the additional memory subsystem is configured to perform a different translation function on the global address to obtain a local physical address of the coherency unit within the additional memory subsystem (Chi's column 6 lines 25-35 discloses that the destination node translates the global address to its local space memory).

As in claim 4, the claim recites wherein the additional memory subsystem is configured to store translation information associated with the coherency unit for several other nodes

included in the plurality of nodes, wherein different translation information is associated with each of the several other nodes (Ang's column 7 lines 3-9 discloses the directory at the home node store/maintain information for addresses that are cached at multiple other nodes).

As in claim 5, Chi's column 5 lines 1-10 discloses wherein each active device included in the plurality of nodes is configured to use at least a portion of the global address of the coherency unit to determine whether a copy of the coherency unit is locally cached by that active device.

As in claim 7, the claim recites wherein no memory subsystem included in an other node of the plurality of nodes maps the global address, wherein an other active device included in the other node is configured to request access to the coherency unit by sending a packet including the global address and translation information associated with the coherency unit in the other node on a network included in the other node, wherein the translation information associated with the coherency unit in the other node indicates that no memory subsystem included in the other node maps the coherency unit. The claim appears to describe the situation, a source processor in the source node (active device in an other node) having a cache miss (no memory subsystem .. maps the global address), it generates the global address and sending out a request/packet to a destination processor in the same other node. Chi's Fig 7, column 5 lines 1-10 discloses the global address is generated by the source processor and sending to the destination processor via the processor bus, within the local space, in the same node.

As in claim 8, the claim recites wherein an other interface included in the other node and coupled to the network is configured to forward the global address to an additional interface included in the additional node in response to receiving the packet (Chi's Fig 1 shows in a ring

topology, the packet can be forwarding from one node to another).

Claim 10 rejected based on the same rationale as of claim 1.

Claim 11 rejected based on the same rationale as of claim 2.

Claim 12 rejected based on the same rationale as of claim 3.

Claim 13 rejected based on the same rationale as of claim 4.

Claim 14 rejected based on the same rationale as of claim 5.

Claim 15 rejected based on the same rationale as of claim 6.

Claim 16 rejected based on the same rationale as of claim 7.

Claim 17 rejected based on the same rationale as of claim 8.

Claim 18 rejected based on the same rationale as of claim 9.

As in claim 19, the claim recites an operating system executing on the active device creating a translation lookaside buffer entry corresponding to the virtual address, wherein the translation lookaside buffer entry includes the global address and the information identifying the translation function, wherein the operating system selects the translation function in order to map the global address to the local physical address within the memory. Chi's column 3 lines 30-45 disclose a translation table with entries includes global address and translation function as shown in Fig 8.

As in claim 20, the claim recites an operating system executing on the active device in the node creating a translation lookaside buffer entry corresponding to a virtual address in response to deciding to replicate the coherency unit to the node from the additional node, wherein the translation lookaside buffer entry corresponding to the virtual address specifies the

global address and the information identifying the translation function. The claim rejected based on the same rationale of claim 19. Chi's column 6 lines 21-28 further discloses the translation is filled by operating system when an application to be run on the system.

Claim 9 rejected under 35 U.S.C. 103(a) as being unpatentable over Chi et al (US 5940870), in view of Ang (US 6678799) as applied to claim 1 and further in view of Arimili et al (US 2002/0112124).

As in claim 9, the claim recites wherein a memory controller included in the memory subsystem is integrated in a same integrated circuit as the processing subsystem. Chi does not describe the claim's aspect of integrated memory controller. However, Arimilli's paragraph 6 discloses a multiple processors system with integrated memory controller circuit. It would have been obvious to one of ordinary skill in the art at the time of invention to include integrated memory controller circuit as suggested by Arimilli in Chi's system to allow fast communication between the processor and the memory controller since they are located in the same chip (Arimilli's page 1 paragraph 6).

Allowable Subject Matter

Claims 6,15 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

(10) Response to Argument

Appellant's arguments in response to the last office action has been fully considered but they are not persuasive. Examiner respectfully traverses Appellant's arguments for the following reasons:

A) Regarding Appellant's arguments at pages 4-8 for the rejections of claims 1-2,4-5 and 7-8 under 35 U.S.C 103(a), the arguments are not persuasive,

First, with respect Appellant remarks at pages 4 to 7, Appellant alleges that Chi does not teach "...translation information identifying a translation function...", "...storing the translation information identifying the translation function..." and "...more over , Fig 8 and its associated description in Chi are directed to only a single transaction function..." as recited in the claim. Appellant further alleges that "the information contained in node ID 114 and partition number 100 does not identify a translation function". However, Appellant has not set forth the differences between Chi's "translation function and the claimed "translation function" and "translation information identifying a translation" as recited in the claim.

Chi's teaching of "the information contained in node ID 114 and partition number 100" identifies a translation function as follows:

Chi's Fig 8 discloses a global address generated by a processor in the node. The Global address (Fig 8: 112) has translation information (node ID and partition number) identifying a translation function (each node uses the global address's translation information), node ID and partition number) to translate and generate physical address corresponding in each node.

Chi's Fig 7 further discloses that **different translation functions are used to select** different address spaces, such as private memory space and near global memory space.

Each address space requires a different translation function. The translation of an address within local space is different than the translation of an address within a near global space or global space. Therefore, different translation functions are required to generate (provide) appropriate addresses corresponding to different address spaces. For example, if the address is within the global address space (i.e data is sent from a source node of a cluster to a destination node of another cluster), the corresponding "global translation function" must lookup AMT for an appropriate value of node ID (a part of the global address). This "node to node lookup" translation function is required to send or receive data from a node in the first cluster to another node in the second cluster by using the global address space and global address (column 6 lines 21-25, cluster interface logic uses node ID of global address). Of course if the address is within the local address space of a node, a different translation function is required which is not the same as the "global translation function" of global address space (i.e source node is the same as destination node, data can simply goes out of the node and come back; see column 5 lines 10-28). Thus, Chi clearly teaches that the node ID is the translation function information identifying a translation function of the global address as recited in the claim. In column 6 lines 22-35, Chi further discloses logic (cluster interface logic) that selects a different translation function corresponding to a different node (receiving node must uses the node ID value of the global address to determine if the address is within its near global address space, and then proceed to remaining steps of stripping node ID, zero receiving partition number etc.). In column 5 lines 28-35, Chi further discloses that the node ID is stored in the ATM table. Therefore Chi's teaching of global address and node ID (corresponding to claim's function translation

information identifying translation function) meets limitations directed to the translation function as claimed.

Regarding Appellant's argument at page 12, "...as evident by the above two citation, item 110 is taught as either a partition number that is a logical node ID or a processor bus address". There appears to be a typographical error in the examiner's statement of the rejection. The examiner apologizes for any confusion the examiner's incorrect citation has cause, but the processor bus address is 100,and the citation to column 5 line 56 is correct.

As discussed above, Chi's teaching of the global address and node ID meet the claim limitations directed to the translation function. Examiner further contends that the logical node ID #110, similarly to node ID #114 provides additional translation functions to translate global address, that is to translate global address to an address belong to a logical partition. In column 5 lines 35 to line 47, Chi teaches a logical node ID of an ATM entry comprising four consecutive locations and four node Ids. These four nodes share a logical partition. Thus, an additional logic partition translation function is required to translate a global address into a device address space in a specific node that is grouped within a specific logical partition. In column 5 lines 47-55, Chi further discloses an alternate scheme to translate the global address to an address belonging to a logical partition, wherein each partition occupies an entry of ATM. Of course a different translation function must be employed in the alternate scheme. Therefore, Chi's teaching of logical node ID #110 also meets the claim's limitations associating with the translation function.

B) Appellant further argues that Chi does not teach "...wherein the additional memory subsystem is configured to perform a different translation function on the global address..." as recited in claim 3. Examiner disagrees. Chi clearly discloses different translation functions must

be applied to memory subsystems in different nodes because memory subsystems of devices in these nodes are organized into different address spaces, and they belong to different logical partitions as discussed at length above in item A.

C) Appellant argues that the rejection of claim 9 is improper for the reasons argued with respect to claim 1. Accordingly, the Board's attention is directed to the examiner's response to these arguments above.

D) Regarding claims 10-12 and 16-20, Appellant repeats the same arguments that are addressed in items A, B above. The Board's attention is respectfully directed to response to these arguments set forth above.

E) Regarding claim 12, Appellant repeats the same arguments that he made with respect to claim 3. Again, the Board's attention is respectfully directed to the examiner's response to these arguments in items A, B and C above.

Finally, Examiner further notes that claims 1-2, 4-5 and 7-8 are directed to a system which comprises a plurality of nodes. And the remaining recitations in the claims merely indicate the intention/capability of the system comprising a plurality of nodes.

(11) Related Proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

/Duc T. Doan/
Duc Doan
Examiner
Art Unit 2188

Conferees:

/Lynne H Browne/
Lynne H Browne
Appeal Practice Specialist, TQAS
Technology Center 2100

HYUNG S. SOUGH
SUPERVISORY PATENT EXAMINER
12/27/07